BHARATHIAR UNIVERSITY: COIMBATORE.

M.Sc. APPLIED ELECTRONICS

(AFFILIATED COLLEGES - Effective from the academic Year 2016-2017)

Revised SCHEME OF EXAMINATIONS – CBCS PATTERN

Sem.	Study Components	Course title	Ins. hrs/ week	Examinations				Credit
				Dur. HRS	CIA	Marks	Total Marks	
I	Paper I	-Microwave and RADAR Navigation Systems	4	3	25	75	100	4
	Paper II	- Microcontroller and its Applications	4	3	25	75	100	4
	Paper III	- Micro Electro Mechanical Systems and Power Electronics	4	3	25	75	100	4
	Paper IV	- Linear ICs and Applications	4	3	25	75	100	4
	Practical I	- General Electronics Lab	5	-	-	-	-	-
	Practical II	- Embedded & VHDL Lab	5	-	-	-	-	-
	Elective Paper I :		4	3	25	75	100	4
II	Paper V	- Embedded Systems	4	3	25	75	100	4
	Paper VI	- VHDL Programming	4	3	25	75	100	4
	Paper VII	- DSP Architecture and Programming	4	3	25	75	100	4
	Paper VIII	-High Performance Communication Networks	4	3	25	75	100	4
	Practical I	- General Electronics Lab	5	4	40	60	100	4
	Practical II	- Embedded & VHDL Lab	5	4	40	60	100	4
	Elective Paper II		4	3	25	75	100	4
III	Paper IX	- Advanced Digital Image Processing	4	3	25	75	100	4
	Paper X	- PC Based System Design	4	3	25	75	100	4
	Paper XI	- Wireless Communication Engineering	4	3	25	75	100	4
	Paper XII	- Nano Electronics and Systems	4	3	25	75	100	4
	Practical III	- PC Hardware Lab	5	4	40	60	100	4
	Practical IV	- DSP and DIP Lab	5	4	40	60	100	4
	Elective Paper III:		4	3	25	75	100	4
	PROJECT WORK & VIVA VOCE		10	-	-	250	250*	10
IV	Elective Practical:		5	4	40	60	100	4
	Total						2250	90

* Project report - 200 marks; Viva-voce – 50 marks

List of Group Elective papers (Colleges can choose any one of the Group papers as electives)

	GROUP A	**GROUP B**	**GROUP C**
Paper I/ Sem I	Web Technologies	Electronic Test Instruments	Basic VLSI Design
Paper II/ Sem II	Relational Data Base Management Systems	Analytical Instrumentation	ASIC Design
Paper III/ Sem III	Linux & Shell Programming	Virtual Instrumentation	VLSI Design Using Verilog
Paper IV/ Sem IV	RDBMS and Linux LAB	Instrumentation Lab	VLSI System Design Lab

Note: 30 days industrial training in an electronics Industry was removed and there is no change in the existing scheme of examination and syllabus of remaining papers.